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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/666,948	09/19/2003	Stephen J. Smith	174/161 Cont	7049

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EXAMINER	
SURYAWANSHI, SURESH	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 09/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/666,948	SMITH ET AL.	
	Examiner	Art Unit	
	Suresh K. Suryawanshi	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *8/10/05 amendments*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,15-18 and 28-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,15-18 and 28* is/are rejected.

7)☐ Claim(s) *29-33* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-4, 15-18 and 28-33 are presented for examination.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claim 28 is rejected under 35 U.S.C. 102(e) as being anticipated by Sharrit et al (US Patent No. 5,999,990; hereinafter Sharrit).

4. As per claim 28, Sharrit teaches a method for managing resources in a computer that contains programmable logic resources that are reconfigurable to optimize the ability of the computer to handle a given application having multiple functions [The communicator includes a controller for dynamically allocating the reconfigurable resource units (col. 1, lines 54-61). The controller includes a resource allocation unit that is operative for allocating the resources of the plurality of RRUs (col. 7, lines 15-33).] comprising :

during run-time [col. 1, lines 54-61; during operation; col. 6, lines 26-29; currently on signal bus], using a virtual computer operating system to autonomously determine whether to use a hardware implementation or a software implementation for a given one of the multiple functions of the given application [The controller, implemented in software, determines whether a signal currently on signal bus will be processed in hardware (in FPGA) or in software (in DSP). Reconfigurable resource units (RRUs) are dynamically altered during operation. Please see col. 1, lines 54-64; col. 2, lines 35-45; col. 6, lines 23-35, 54-57.].

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sharrit et al (US Patent No. 5,999,990; hereinafter Sharrit) in view of Vernon et al (EP 0 801 351 A2; hereinafter Vernon).

7. As per claim 1, Sharrit discloses a reconfigurable computer system comprising:

at least one programmable logic resource [col. 1, lines 54-59; a plurality of reconfigurable resource units (RRUs)];

programmable logic coupled to the central processing unit [Fig. 3, 4; col. 2, lines 55-58; col. 5, lines 36-38, 58-60], wherein the programmable logic is reconfigurable to optimize the ability of the computer system to handle a given application [col. 1, lines 54-61; col. 2, lines 35-45; col. 6, lines 23-35]; and

a secondary storage device that stores configuration data for the programmable logic, wherein the secondary storage device is a mass storage device [col. 5, lines 33-57; a hard disk].

Sharrit does not expressly disclose about at least one programmable logic resource that is at least partially configured as a central processing unit. But a routineer in the art would know that a programmable logic resource could be implemented or programmed to function as a central processing unit. However, Vernon explicitly discloses implementing at least one programmable logic resource as a central processing unit [col. 3, lines 5-10; FPGA is configured to provide the functions of a microprocessor]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references as both are related to programmable logic circuits and their implementations. Moreover, one can clearly see the benefit of utilizing programmable logic resources as they can be readily

reconfigured as needed according to the current system requirements. Further, there is a benefit of having simpler and smaller circuit boards for producing small and convenient user devices.

8. As per claim 2, Sharrit discloses that the system further comprising non-volatile memory coupled to the programmable logic [col. 5, lines 33-56; a hard disk drive].

9. As per claim 3, Sharrit discloses that the system further comprising random-access memory coupled to the programmable logic [col. 5, lines 33-56; RAM].

10. As per claim 4, Sharrit discloses that the system further comprising input-output circuitry [Fig. 1; col. 2, lines 28-31; input/output port].

11. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kean (US Patent No. 5,705,938; hereinafter Kean938) in view of Kean (US Patent No. 5,469,003; hereinafter Kean003).

12. As per claim 15, Kean938 discloses a programmable switch for a field programmable gate array (FPGA) allows a user to reconfigure or partly reconfigure the FPGA from within the FPGA. Further, Kean938 expressly discloses swapping configuration data between a secondary storage device and the programmable logic resource during programmable logic resource allocation [col. 11, lines 49-59; "swapping in" and "swapping out" with an external memory].

Kean938 does not expressly disclose that the external memory is a mass storage device. But a routineer in the art would recognize that a common external memory is usually a mass storage device. However, Kean003 clearly discloses about storing the configuration data in a disk file [col. 38, lines 29-33; disk files are stored in a mass storage device]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references as both are directed to configure a field programmable gate array (FPGA). Moreover, it is clearly beneficial to utilize a mass storage device in the system where swapping is performed regularly for many different applications because the mass storage device can provide plenty of storage spacing.

13. Claim 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kean (US Patent No. 5,705,938; hereinafter Kean938) in view of Kean (US Patent No. 5,469,003; hereinafter Kean003) and further in view of Vernon et al (EP 0 801 351 A2; hereinafter Vernon).

14. As per claims 16-18, Kean938 and Kean003 disclose the invention substantially. Kean938 and Kean003 do not expressly disclose about a central processing unit may be implemented on or with one programmable logic device or a microprocessor or partially implemented on a microprocessor and that is partially implemented on a programmable logic device. But a routineer in the art would know that a programmable logic resource could be implemented or programmed to function as a central processing unit. However, Vernon explicitly discloses implementing at least one programmable logic resource as a central processing unit [col. 3, lines 5-10; FPGA is configured to provide the functions of a microprocessor; col. 3, lines 33-35; different possible combinations]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references as they are related to programmable logic circuits and their implementations. Moreover, one can clearly see the benefit of utilizing programmable logic resources as they can be readily reconfigured as needed and eliminating the need of custom chip design.

Allowable Subject Matter

15. Claims 29-33 are objected to as being dependent upon a rejected base claim 28, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

16. Applicant's arguments with respect to claims 1-4, 15-18 and 28-33 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suresh K. Suryawanshi whose telephone number is 571-272-3668. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sks
September 13, 2005

THOMAS LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER